UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,408	08/18/2001	Russell Dickerson	230074-0237	4316

7590 11/24/2004

Ted R. Rittmaster
Foley & Lardner
Suite 3500
2029 Century Park East
Los Angeles, CA 90067-3021

EXAMINER	
CHAI, LONGBIT	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,408	DICKERSON ET AL.	
	Examiner	Art Unit	
	Longbit Chai	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-07-2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. No claim for priority has been made in this application.

The effective filing date for the subject matter defined in the pending claims in this application is 8/18/2001.

Drawings

2. Figure 3A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraph of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 4, 6 – 9, 13 – 16 and 19 – 23 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Nasu (Patent Number: 6088262), hereinafter referred to as Nasu.

As per claim 1 and 13, Nasu teaches a method for obstructing access to a secure area of a semiconductor device comprising:

providing a control signal indicating that the semiconductor device has entered a secure mode (Nasu: see for example, Column 9 Line 20, Column 2 Line 51 – 55 and Figure 12A and Figure 15A: Read protection signal is an equivalent to the control signal); and obstructing access to the secure area utilizing the control signal (Nasu: see for example, Column 9 Line 12 – 15).

As per claim 2 and 14, Nasu teaches the claimed invention as described above (see claim 1 and 13 respectively). Nasu further teaches obstructing access to the secure area comprises gating another signal with the control signal (Nasu: see for example, Figure 12A and Figure 15A).

As per claim 3, Nasu teaches the claimed invention as described above (see claim 1). Nasu further teaches obstructing access to the secure area comprises is selecting a multiplexer channel with the control signal (Nasu: see for example, Figure 12A and Figure 15A: a multiplex circuit is an obvious design variant from the AND gate composition circuit).

As per claim 4, Nasu teaches the claimed invention as described above (see claim 1). Nasu further teaches obstructing access to the secure area comprises enabling another circuit with the control signal (Nasu: see for example, Figure 12A, Figure 15A and column 2 Line 24 – 27).

As per claim 6, Nasu teaches the claimed invention as described above (see claim 1). Nasu further teaches providing a control signal further comprises decoding a plurality of signals to generate the control signal (Nasu: see for example, column 2 Line 51 – 57).

As per claim 7, Nasu teaches the claimed invention as described above (see claim 1). Nasu further teaches the control signal transitions from a first logic state to a second logic state when the semiconductor device enters the secure mode (Nasu: see for example, Figure 15B).

As per claim 8, Nasu teaches the claimed invention as described above (see claim 7). Nasu further teaches the first logic state is a logic high and the second logic state is a logic low (Nasu: see for example, Figure 15B).

As per claim 9, Nasu teaches the claimed invention as described above (see claim 7). Nasu further teaches the first logic state is a logic low and the second logic state is a logic high (Nasu: see for example, Figure 15B).

As per claim 15, Nasu teaches the claimed invention as described above (see claim 14). Nasu further teaches the logic gate is an AND gate having a first input connected to the first circuit such that the first input responds to the control signal (Nasu: see for example, Column 2 Line 51 – 55 and Figure 12A); a second input connected to a circuit supplying output data (Nasu: see for example, Figure 12A Element 805); and an output connected to a port of the semiconductor device (Nasu: see for example, Figure 10A).

As per claim 16, Nasu teaches the claimed invention as described above (see claim 13). Nasu further teaches second circuit is a multiplexer (Nasu: see for example, Figure 12A and Figure 15A: a multiplex circuit is an obvious design variant from the AND gate composition circuit).

As per claim 19, Nasu teaches the claimed invention as described above (see claim 13). Nasu further teaches the secure area comprises memory (Nasu: see for example, Figure 16).

As per claim 20, Nasu teaches the claimed invention as described above (see claim 13). Nasu further teaches the semiconductor device is an application specific integrated circuit (Nasu: see for example, Figure 16).

As per claim 21, Nasu teaches the claimed invention as described above (see claim 13). Nasu further teaches the first circuit is a microprocessor core (Nasu: see for example, Column 2 Line 51 – 57).

As per claim 22, Nasu teaches the claimed invention as described above (see claim 13). Nasu further teaches the the first circuit is a decoder (Nasu: see for example, Column 2 Line 51 – 57).

As per claim 23, Nasu teaches the claimed invention as described above (see claim 15). Nasu further teaches the output is buffered before connecting to the port (Nasu: see for example, Column 3 Line 62 – 63 and Figure 10A).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 5, 10 11, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nasu (Patent Number: 6088262), hereinafter referred to as Nasu, in view of Applicant Admitted Prior-art (Publication Number: US 2003/0212897 A1), hereinafter referred to as AAP.

As per claim 24, Nasu teaches system for obstructing access to a secure area of a semiconductor device comprising:

an AND gate having a first input connected to the control line, a second input connected to the data output line, and an output connected to an input of a buffer (Nasu: see for example, Column 9 Line 16 – 22, Figure 10A and Figure 12A).

Nasu does not teach a port implemented in the semiconductor device for connecting to an in-circuit emulator, wherein a line on the port is also connected to an output of the buffer.

AAP teaches a port implemented in the semiconductor device for connecting to an in-circuit emulator, wherein a line on the port is also connected to an output of the buffer (AAP: see for example, Figure 3A Element 22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of AAP within the system of Nasu because (a) AAP teaches the semiconductor device includes buffers/drivers for sending output data externally (AAP: see for example, Paragraph [0030] 5th sentence) and (b) Nasu teaches protecting data from being read out from the outside for secure data and thereby enhancing the overall system security (Nasu: see for example, Column 1 Line 55 – 57).

Therefore, Nasu as modified further teaches:

a microprocessor core (AAP: see for example, Figure 3A Element 40); a decoder connected to an output of the microprocessor core (AAP: see for example, Figure 3A Element 46); a control line connected to an output of the decoder; a circuit for supplying output data; a data output line connected to an output of the circuit for supplying output data (AAP: see for example, Figure 3A Element 48).

when the in-circuit emulator requests access to the secure area, the microprocessor core generates microprocessor signals for decoding by the decoder (AAP: see for example, Paragraph [0030] 1st – 5th sentences) & (Nasu: see for example, Column 1 Line 55 – 57), and

wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the AND gate outputs an obstructing signal to obstruct access by the in-circuit emulator to the secure area (AAP: see for example, Paragraph [0030] 1st – 5th sentences) & (Nasu: see for example, Column 1 Line 55 – 57).

As per claim 5, Nasu teaches the claimed invention as described above (see claim 1). Nasu does not teach the secure area is used in connection with data encryption.

AAP teaches the secure area is used in connection with data encryption (AAP: see for example, Paragraph [0004] – Last sentence).

See the same rationale of combination applied here as above in rejecting the claim 24.

As per claim 10, Nasu teaches the claimed invention as described above (see claim 1). Nasu does not teach connecting an in-circuit emulator to the semiconductor device; and generating a command from the in-circuit emulator to the semiconductor device, wherein the command requests access to the secure area of the semiconductor.

AAP teaches connecting an in-circuit emulator to the semiconductor device; and generating a command from the in-circuit emulator to the semiconductor device, wherein the command requests access to the secure area of the semiconductor (AAP: see for example, Paragraph [0006] and [0007]).

See the same rationale of combination applied here as above in rejecting the claim 24.

As per claim 11, Nasu as modified teaches the claimed invention as described above (see claim 10). Nasu as modified further teaches the semiconductor device

enters the secure mode when the in-circuit emulator is connected to the semiconductor device (Nasu: see for example, Column 1 Line 55 – 57).

As per claim 17, Nasu teaches the claimed invention as described above (see claim 13). Nasu doe not teach comprising a port for an in-circuit emulator.

AAP teaches comprising a port for an in-circuit emulator (AAP: see for example, Figure 3A).

See the same rationale of combination applied here as above in rejecting the claim 24.

As per claim 18, Nasu as modified teaches the claimed invention as described above (see claim 17). Nasu as modified further teaches the semiconductor device enters the secure mode when the in-circuit emulator is connected to the port (Nasu: see for example, Column 9 Line 16 – 22, Figure 10A and Figure 12A) & (AAP: see for example, Figure 3A Element 22).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nasu (Patent Number: 6088262), hereinafter referred to as Nasu, in view of Applicant Admitted Prior-art (Publication Number: US 2003/0212897 A1), hereinafter referred to as AAP, and in view of Boyce (Patent Number: 4796258), hereinafter referred to as Boyce.

As per claim 12, Nasu as modified teaches the claimed invention as described above (see claim 10). Nasu as modified does not teach the command is a software interrupt.

Boyce teaches the command is a software interrupt (Boyce: see for example, Column 3 Line 61 – 68: Boyce teaches a software interrupt is generated from a microprocessor debug tool which has an emulator upon detection of a user specified event – i.e. including a user command).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Boyce within the system of Nasu as modified because Boyce teaches providing a microprocessor debug tool which can effectively monitor the system operation (Boyce: see for example, Column 1 Line 44 – 47).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 703-305-0710. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R Sheikh can be reached on 571 272-3795 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Longbit Chai
Examiner
Art Unit 2131

LBC

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100